

# MC74LCX16244

## Low-Voltage CMOS 16-Bit Buffer

### With 5 V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

The MC74LCX16244 is a high performance, non-inverting 16-bit buffer operating from a 2.3 to 3.6 V supply. The device is nibble controlled. Each nibble has separate Output Enable inputs which can be tied together for full 16-bit operation. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A  $V_I$  specification of 5.5 V allows MC74LCX16244 inputs to be safely driven from 5.0 V devices. The MC74LCX16244 is suitable for memory address driving and all TTL level bus oriented transceiver applications.

The 4.5 ns maximum propagation delays support high performance applications. Current drive capability is 24 mA at the outputs. The Output Enable ( $\overline{OEn}$ ) inputs, when HIGH, disable the outputs by placing them in a HIGH Z condition.

The MC74LCX16244 contains sixteen non-inverting buffers with 3-state 5.0 V-tolerant outputs. The device is nibble controlled with each nibble functioning identically, but independently. The control pins may be tied together to obtain full 16-bit operation. The 3-state outputs are controlled by an Output Enable ( $\overline{OEn}$ ) input for each nibble. When  $\overline{OEn}$  is LOW, the outputs are on. When  $\overline{OEn}$  is HIGH, the outputs are in the high impedance state.

#### Features

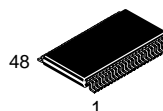
- Designed for 2.3 V to 3.6 V  $V_{CC}$  Operation
- 4.5 ns Maximum  $t_{pd}$
- 5.0 V Tolerant – Interface Capability With 5.0 V TTL Logic
- Supports Live Insertion and Withdrawal
- $I_{OFF}$  Specification Guarantees High Impedance When  $V_{CC} = 0$  V
- LVTTL Compatible
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (20  $\mu$ A)  
Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500 mA
- ESD Performance: Human Body Model >2000 V;  
Machine Model >200 V
- All Devices in Package TSSOP are Inherently Pb-Free\*

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



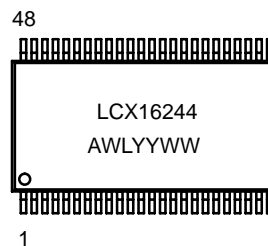
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TSSOP-48  
DT SUFFIX  
CASE 1201

#### MARKING DIAGRAM



A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

# MC74LCX16244

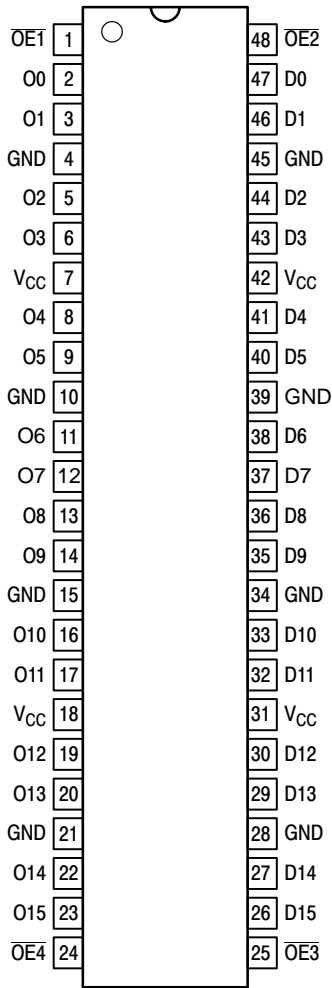


Figure 1. Pinout: 48-Lead (Top View)

Table 1. PIN NAMES

Pins	Function
$\overline{OE}_n$	Output Enable Inputs
D0–D15	Inputs
O0–O15	Outputs

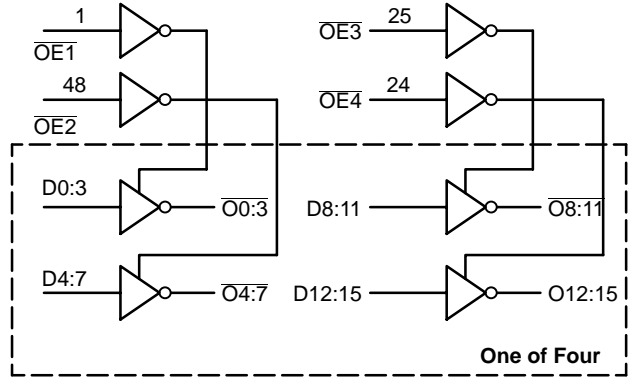


Figure 2. Logic Diagram

## TRUTH TABLE

$\overline{OE}_1$	D0:3	O0:3	$\overline{OE}_2$	D4:7	O4:7	$\overline{OE}_3$	D8:11	O8:11	$\overline{OE}_4$	D12:15	O12:15
L	L	L	L	L	L	L	L	L	L	L	L
L	H	H	L	H	H	L	H	H	L	H	H
H	X	Z	H	X	Z	H	X	Z	H	X	Z

H = High Voltage Level  
 L = Low Voltage Level  
 Z = High Impedance State  
 X = High or Low Voltage Level and Transitions Are Acceptable; for  $I_{CC}$  reasons, DO NOT FLOAT Inputs.

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## ORDERING INFORMATION

Device	Package	Shipping†
MC74LCX16244DT	TSSOP-48*	39 Units / Rail
MC74LCX16244DTR2	TSSOP-48*	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*This package is inherently Pb-Free.

## MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Unit
$V_{CC}$	DC Supply Voltage	-0.5 to +7.0		V
$V_I$	DC Input Voltage	$-0.5 \leq V_I \leq +7.0$		V
$V_O$	DC Output Voltage	$-0.5 \leq V_O \leq +7.0$	Output in 3-State	V
		$-0.5 \leq V_O \leq V_{CC} + 0.5$	Output in HIGH or LOW State (Note 1)	V
$I_{IK}$	DC Input Diode Current	-50	$V_I < \text{GND}$	mA
$I_{OK}$	DC Output Diode Current	-50	$V_O < \text{GND}$	mA
		+50	$V_O > V_{CC}$	mA
$I_O$	DC Output Source/Sink Current	$\pm 50$		mA
$I_{CC}$	DC Supply Current Per Supply Pin	$\pm 100$		mA
$I_{GND}$	DC Ground Current Per Ground Pin	$\pm 100$		mA
$T_{STG}$	Storage Temperature Range	-65 to +150		°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1.  $I_O$  absolute maximum rating must be observed.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	
$V_{CC}$	Supply Voltage	Operating	2.0	2.5, 3.3	3.6	V
		Data Retention Only	1.5	2.5, 3.3	3.6	
$V_I$	Input Voltage	0		5.5	V	
$V_O$	Output Voltage (HIGH or LOW State) (3-State)	0		$V_{CC}$	V	
		0		5.5		
$I_{OH}$	HIGH Level Output Current	$V_{CC} = 3.0 \text{ V} - 3.6 \text{ V}$		-24	mA	
		$V_{CC} = 2.7 \text{ V} - 3.0 \text{ V}$		-12		
		$V_{CC} = 2.3 \text{ V} - 2.7 \text{ V}$		-8		
$I_{OL}$	LOW Level Output Current	$V_{CC} = 3.0 \text{ V} - 3.6 \text{ V}$		+24	mA	
		$V_{CC} = 2.7 \text{ V} - 3.0 \text{ V}$		+12		
		$V_{CC} = 2.3 \text{ V} - 2.7 \text{ V}$		+8		
$T_A$	Operating Free-Air Temperature	-40		+85	°C	
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, $V_{IN}$ from 0.8 V to 2.0 V, $V_{CC} = 3.0 \text{ V}$	0		10	ns/V	

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## DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T <sub>A</sub> = -40°C to +85°C		Unit
			Min	Max	
V <sub>IH</sub>	HIGH Level Input Voltage (Note 2)	2.3 V ≤ V <sub>CC</sub> ≤ 2.7 V	1.7		V
		2.7 V ≤ V <sub>CC</sub> ≤ 3.6 V	2.0		
V <sub>IL</sub>	LOW Level Input Voltage (Note 2)	2.3 V ≤ V <sub>CC</sub> ≤ 2.7 V		0.7	V
		2.7 V ≤ V <sub>CC</sub> ≤ 3.6 V		0.8	
V <sub>OH</sub>	HIGH Level Output Voltage	2.3 V ≤ V <sub>CC</sub> ≤ 3.6 V; I <sub>OL</sub> = 100 μA	V <sub>CC</sub> - 0.2		V
		V <sub>CC</sub> = 2.3 V; I <sub>OH</sub> = -8 mA	1.8		
		V <sub>CC</sub> = 2.7 V; I <sub>OH</sub> = -12 mA	2.2		
		V <sub>CC</sub> = 3.0 V; I <sub>OH</sub> = -18 mA	2.4		
		V <sub>CC</sub> = 3.0 V; I <sub>OH</sub> = -24 mA	2.2		
V <sub>OL</sub>	LOW Level Output Voltage	2.3 V ≤ V <sub>CC</sub> ≤ 3.6 V; I <sub>OL</sub> = 100 μA		0.2	V
		V <sub>CC</sub> = 2.3 V; I <sub>OL</sub> = 8 mA		0.6	
		V <sub>CC</sub> = 2.7 V; I <sub>OL</sub> = 12 mA		0.4	
		V <sub>CC</sub> = 3.0 V; I <sub>OL</sub> = 16 mA		0.4	
		V <sub>CC</sub> = 3.0 V; I <sub>OL</sub> = 24 mA		0.55	
I <sub>I</sub>	Input Leakage Current	2.3 V ≤ V <sub>CC</sub> ≤ 3.6 V; 0 V ≤ V <sub>I</sub> ≤ 5.5 V		±5.0	μA
I <sub>OZ</sub>	3-State Output Current	2.3 ≤ V <sub>CC</sub> ≤ 3.6 V; 0V ≤ V <sub>O</sub> ≤ 5.5 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>		±5.0	μA
I <sub>OFF</sub>	Power-Off Leakage Current	V <sub>CC</sub> = 0 V; V <sub>I</sub> or V <sub>O</sub> = 5.5 V		10	μA
I <sub>CC</sub>	Quiescent Supply Current	2.3 ≤ V <sub>CC</sub> ≤ 3.6 V; V <sub>I</sub> = GND or V <sub>CC</sub>		20	μA
		2.3 ≤ V <sub>CC</sub> ≤ 3.6 V; 3.6 ≤ V <sub>I</sub> or V <sub>O</sub> ≤ 5.5 V		±20	μA
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	2.3 ≤ V <sub>CC</sub> ≤ 3.6 V; V <sub>IH</sub> = V <sub>CC</sub> - 0.6 V		500	μA

2. These values of V<sub>I</sub> are used to test DC electrical characteristics only.

## AC CHARACTERISTICS t<sub>R</sub> = t<sub>F</sub> = 2.5 ns; R<sub>L</sub> = 500 Ω

Symbol	Parameter	Waveform	T <sub>A</sub> = -40°C to +85°C						Unit
			V <sub>CC</sub> = 3.3 V ± 0.3 V C <sub>L</sub> = 50 pF		V <sub>CC</sub> = 2.7 V C <sub>L</sub> = 50 pF		V <sub>CC</sub> = 2.5 V ± 0.2 V C <sub>L</sub> = 30 pF		
			Min	Max	Min	Max	Min	Max	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Input to Output	1	1.5 1.5	4.5 4.5	1.5 1.5	5.2 5.2	1.5 1.5	5.4 5.4	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time to High and Low Level	2	1.5 1.5	5.5 5.5	1.5 1.5	6.3 6.3	1.5 1.5	7.2 7.2	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time From High and Low Level	2	1.5 1.5	5.4 5.4	1.5 1.5	5.7 5.7	1.5 1.5	6.5 6.5	ns
t <sub>OSSL</sub> t <sub>OSLH</sub>	Output-to-Output Skew (Note 3)			1.0 1.0					ns

3. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSSL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>); parameter guaranteed by design.

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## DYNAMIC SWITCHING CHARACTERISTICS

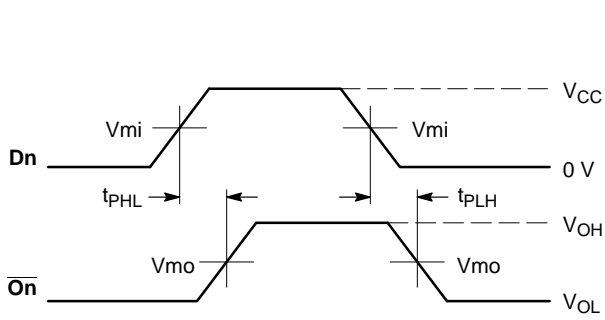
Symbol	Characteristic	Condition	T <sub>A</sub> = +25°C			Unit
			Min	Typ	Max	
V <sub>OLP</sub>	Dynamic LOW Peak Voltage (Note 4)	V <sub>CC</sub> = 3.3 V, C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3 V, V <sub>IL</sub> = 0 V		0.8		V
		V <sub>CC</sub> = 2.5 V, C <sub>L</sub> = 30 pF, V <sub>IH</sub> = 2.5 V, V <sub>IL</sub> = 0 V		0.6		V
V <sub>OLV</sub>	Dynamic LOW Valley Voltage (Note 4)	V <sub>CC</sub> = 3.3 V, C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3 V, V <sub>IL</sub> = 0 V		-0.8		V
		V <sub>CC</sub> = 2.5 V, C <sub>L</sub> = 30 pF, V <sub>IH</sub> = 2.5 V, V <sub>IL</sub> = 0 V		-0.6		V

4. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

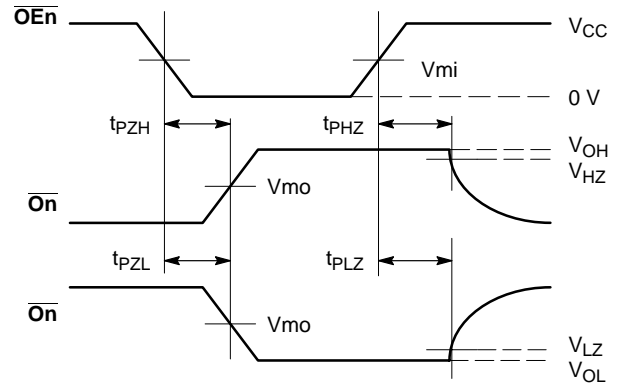
## CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = 3.3 V, V <sub>I</sub> = 0 V or V <sub>CC</sub>	7	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>CC</sub> = 3.3 V, V <sub>I</sub> = 0 V or V <sub>CC</sub>	8	pF
C <sub>PD</sub>	Power Dissipation Capacitance	10 MHz, V <sub>CC</sub> = 3.3 V, V <sub>I</sub> = 0 V or V <sub>CC</sub>	20	pF

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**WAVEFORM 1 – PROPAGATION DELAYS**  
 $t_R = t_F = 2.5 \text{ ns}$ , 10% to 90%;  $f = 1 \text{ MHz}$ ;  $t_W = 500 \text{ ns}$

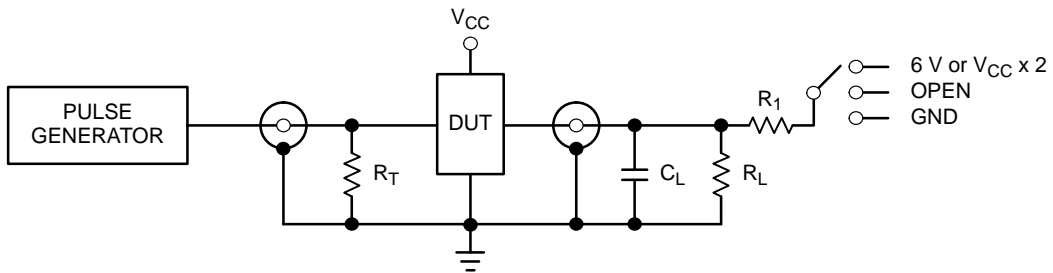


**WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES**  
 $t_R = t_F = 2.5 \text{ ns}$ , 10% to 90%;  $f = 1 \text{ MHz}$ ;  $t_W = 500 \text{ ns}$

**Figure 3. AC Waveforms**

**Table 2. AC WAVEFORMS**

Symbol	V <sub>CC</sub>		
	3.3 V ± 0.3 V	2.7 V	2.5 V ± 0.2 V
V <sub>mi</sub>	1.5 V	1.5 V	V <sub>CC</sub> / 2
V <sub>mo</sub>	1.5 V	1.5 V	V <sub>CC</sub> / 2
V <sub>HZ</sub>	V <sub>OL</sub> + 0.3 V	V <sub>OL</sub> + 0.3 V	V <sub>OL</sub> + 0.15 V
V <sub>LZ</sub>	V <sub>OH</sub> - 0.3 V	V <sub>OH</sub> - 0.3 V	V <sub>OH</sub> - 0.15 V



**Figure 4. Test Circuit**

**Table 3. TEST CIRCUIT**

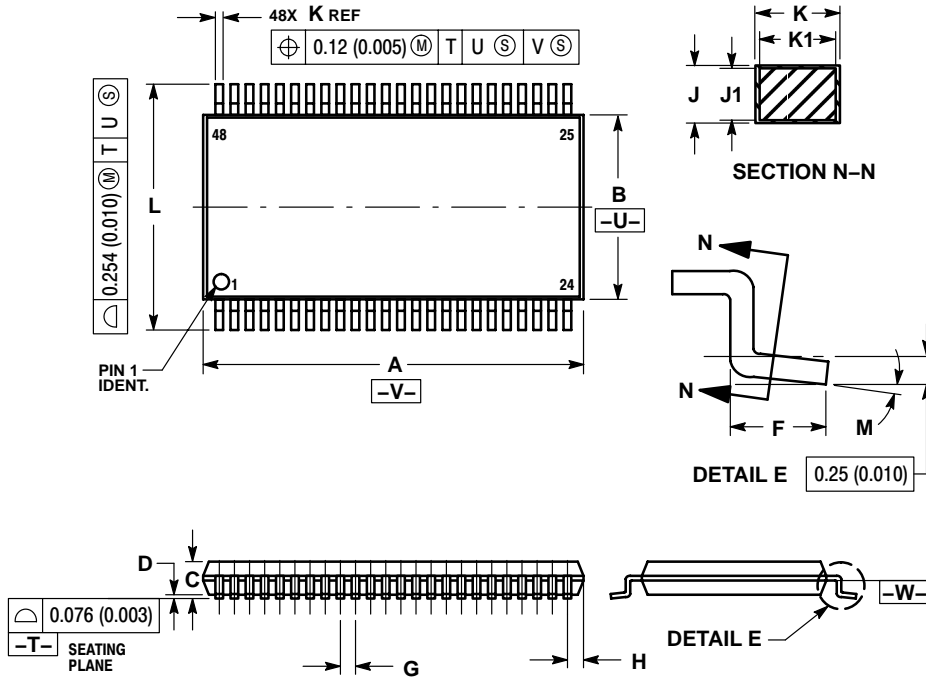
TEST	SWITCH
t <sub>PLH</sub> , t <sub>PHL</sub>	Open
t <sub>PZL</sub> , t <sub>PLZ</sub>	6 V at V <sub>CC</sub> = 3.3 ± 0.3 V 6 V at V <sub>CC</sub> = 2.5 ± 0.2 V
Open Collector/Drain t <sub>PLH</sub> and t <sub>PHL</sub>	6 V
t <sub>PZH</sub> , t <sub>PHZ</sub>	GND

C<sub>L</sub> = 50 pF at V<sub>CC</sub> = 3.3 ± 0.3 V or equivalent (includes jig and probe capacitance)  
 C<sub>L</sub> = 30 pF at V<sub>CC</sub> = 2.5 ± 0.2 V or equivalent (includes jig and probe capacitance)  
 R<sub>L</sub> = R<sub>1</sub> = 500 Ω or equivalent  
 R<sub>T</sub> = Z<sub>OUT</sub> of pulse generator (typically 50 Ω)

# MC74LCX16244

## PACKAGE DIMENSIONS

TSSOP-48  
DT SUFFIX  
CASE 1201-01  
ISSUE A



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.40	12.60	0.488	0.496
B	6.00	6.20	0.236	0.244
C	---	1.10	---	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.50	BSC	0.0197	BSC
H	0.37	---	0.015	---
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.17	0.27	0.007	0.011
K1	0.17	0.23	0.007	0.009
L	7.95	8.25	0.313	0.325
M	0°	8°	0°	8°

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